



Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)		TY. DKT. NO. 5181-97900 APPLICANT: Cavanagh, et al. FILING DATE: November 9, 2001	SERIAL NO. 10/010,572 GROUP: 2123 RECEIVED FEB 28 2002 Hardware Description Language Center 2100
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
<i>Copy</i>	A28	"Rule Base Driven Conversion of an Object Oriented Design Structure Into Standard Hardware Description Languages," Verschueren, A.C., IEEE Xplore, appears in Euromicro Conference, 1998, Proceedings, 24 th , vol. 1, August 25, 1998, pages 42-45.	
<i>Copy</i>	A29	"Modeling Communication with Objective VHDL," Putzke, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings., 1998 International, March 16, 1998, pages 83-89.	
<i>Copy</i>	A30	"A Procedural Language Interface for VHDL and its Typical Applications," Martinolle, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings., 1998 International, March 16, 1998, pages 32-38.	
<i>Copy</i>	A31	"The Verilog Procedural Interface for the Verilog Hardware Description Language," Dawson, et al., IEEE Xplore, appears in Verilog HDL Conference, 1996, Proceedings., 1996 International, February 26, 1996, pages 17-23.	
<i>Copy</i>	A32	"An Integrated Environment for HDL Verification," York, et al., IEEE Xplore, appears in Verilog HDL Conference, 1995, Proceedings., 1995 International, March 27, 1995, pages 9-18.	
<i>Copy</i>	A33	"The PowerPC 603 C++ Verilog Interface Model," Voith, R.P., IEEE Xplore, appears in Compcon Spring '94, Digest of Papers, Feb. 28, 1994, pages 337-340.	
<i>Copy</i>	A34	"Networked Object Oriented Verification with C++ and Verilog, Dearth, et al., IEEE, XP-002144328, 1998, 4 pages.	
<i>Copy</i>	A35	Patent Abstracts of Japan, publication no. 10326835, published December 8, 1998.	
<i>Copy</i>	A36	Patent Abstracts of Japan, publication no. 10049560, published February 20, 1998.	
<i>Copy</i>	A37	Patent Abstracts of Japan, publication no. 10340283, published December 22, 1998.	
<i>Copy</i>	A38	Patent Abstracts of Japan, publication no. 07254008, published October 3, 1995.	
<i>Copy</i>	A39	"Multiprocessing Verilog Simulator Exploits the Parallel Nature of HDLs." Lisa Maliniak, Electronic Design, Abstract, May 30, 1994, 1 page.	
<i>Copy</i>	A40	"It's A Multithreaded World, Part I," Charles J. Northrup, BYTE, May 1992, 7 pages.	
<i>Copy</i>	A41	"It's a Multithreaded World, Part 2," Charles J. Northrup, BYTE, June 1992, pp. 351-356.	
<i>Copy</i>	A42	"Weaving a Thread," Shashi Prasad, BYTE, October 1995, pp. 173-174.	
<i>Copy</i>	A43	"Making Sense of Collaborative Computing," Mark Gibbs, Network World Collaboration, January 10, 1994, 4 pages.	
<i>Copy</i>	A44	"Parallel Logic Simulation of VLSI Systems," Bailey, et al., ACM Computing Surveys, Vol. 26, No. 3, September 1994, pp. 255-294.	
<i>Copy</i>	A45	"Multithreaded Languages for Scientific and Technical Computing," Cherri M. Pancake, Proceedings of the IEEE, Vol. 81, No. 2, February 1993, pp. 288-304.	
<i>Copy</i>	A46	"Distributed Simulation Architecture, SW Environment, Enterprise Server Products," Purdue EE400 Presentation by Freyensee and Frankel, November 9, 2000, 13 pages.	

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